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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,735	12/31/2003	Duc V. Ho	MICS:0119 (03-0188)	1832
7590 12/23/2005			EXAMINER	
Michael G. Fletcher Fletcher Yoder			NGUYEN, MATTHEW VAN	
P.O. Box 692289			ART UNIT	PAPER NUMBER
Houston, TX	77269-2289	2838		

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applica	ition No.	Applicant(s)		
Office Action Summary		10/750	,735	HO ET AL.		
		Examir	ier	Art Unit		
		MATTH	EW V. NGUYEN	2838		
The MAILING I	DATE of this communi	cation appears on	the cover sheet wit	h the correspondence add	dress	
A SHORTENED STA WHICHEVER IS LON - Extensions of time may be after SIX (6) MONTHS from - If NO period for reply is spe - Failure to reply within the si Any reply received by the Co	NGER, FROM THE MA available under the provisions on the mailing date of this commit	AILING DATE OF of 37 CFR 1.136(a). In no unication. Intutory period will apply and will, by statute, cause the a	THIS COMMUNIC event, however, may a re d will expire SIX (6) MONT application to become ABA	ply be timely filed I'HS from the mailing date of this co ANDONED (35 U.S.C. § 133).		
Status						
2a) This action is <b>F</b> 3) Since this appli		b)⊠ This action is or allowance exce	non-final.  pt for formal matte	ers, prosecution as to the .11, 453 O.G. 213.	merits is	
Disposition of Claims						
4a) Of the abov 5) ☐ Claim(s) 6) ☒ Claim(s) 1-13,1 7) ☒ Claim(s) 14 and 8) ☐ Claim(s)  Application Papers 9) ☐ The specificatio 10) ☒ The drawing(s) Applicant may no Replacement drawing	15-36 and 38-40 is/are d 37 is/are objected to are subject to restrict on is objected to by the filed on 31 December of request that any objective in isolation in the filed on including sheet(s) including	e withdrawn from or rejected.  ion and/or election examiner.  2003 is/are: a)  tion to the drawing(sthe correction is req	accepted or b)	objected to by the Exam ce. See 37 CFR 1.85(a). s) is objected to. See 37 CF Office Action or form PT	FR 1.121(d).	
Priority under 35 U.S.C.	. § 119					
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>						
Attachment(s)  1) Notice of References Cit 2) Notice of Draftsperson's 3) Information Disclosure S Paper No(s)/Mail Date 1	Patent Drawing Review (Ptatement(s) (PTO-1449 or I		Paper No(s	ummary (PTO-413) )/Mail Date formal Patent Application (PTC 	)-152)	

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1. The disclosure should be carefully reviewed and ensure that any and all grammatical, idiomatic, and spelling or other minor errors are corrected.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 13, 15-17 and 21-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Khosrowpour (U.S. Pat. No. 6,202,115).

With regard to claims 1-8, 13, 15-17 and 21-30, Khosrowpour shows a bus bridge system and a method thereof comprising a processor (as in computer network, col. 1, line 13), a memory device (Fig. 1) coupled to the processor including a first voltage bus (101), a second voltage bus (102), a bridge circuit (110, 120) coupled between the first voltage bus and the second voltage bus for receiving an input signal (112, 122) such as connecting the first voltage bus to the second voltage bus if the input signal is a first control signal (112) and isolating the first voltage bus from the second voltage bus if the input signal is a second control signal (122) (see col. 4, lines 14-27, noting that first and second control signals 112, 122 as in drawings, but mistakenly listed as 115 and 125, respectively), the memory device further including a DRAM device and SRAM device (col. 5, line 21), the processor being coupled to a communication port to communicate with an input/output device, to a user interface, or to a display

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presenting information to a user, and to the power supply being externally to the memory, the first voltage being a voltage supply bus for periphery circuitry and the second voltage bus being a voltage supply bus for array circuitry (col. 1, lines 11-50, col. 2, lines 28-68).

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 18, 19, 31, 33, 36 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour in view of Nakagawa et al. (U.S. Pat. No. 6,643,713).

With regard to claims 9, 10, 18, 19, 31, 33, 36 and 38-40, Khosrowpour shows a bus bridge system and a method thereof comprising all the claimed subject matter as discussed in the subparagraph 2 above, except for a plurality of power amplifiers coupled to the first voltage bus.

Nakagawa et al. (Fig. 2) disclose an internal connection for a communication system in which a power amplifier (212) is included.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the power amplifier as shown in Nakagawa et al. into the bus bridge system of Khosrowpour for the purpose of enhancing the power to the voltage bus.

4. Claims 11, 12, 20 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour in view of Liu (U.S. Pat. No. 6,940,340).

With regard to claims 11, 12, 20 and 32, Khosrowpour shows a bus bridge system and a method thereof comprising all the claims subject matter as discussed in the subparagraph 2 above, except for a voltage detector coupled to the first and second voltage buses.

Liu (Fig. 3) discloses a bus circuit in which a voltage detector (18) is connected to a voltage bus.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the voltage detector being connected to a voltage bus as shown in Liu into the bus bridge system of Khosrowpour for the purpose of determining the voltage on the voltage bus of the system.

5. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour in view of Nakagawa et al. as applied to claims 33 above, and further in view of Liu.

With regard to claims 34 and 35, Khosrowpour and Nakagawa et al. show a bus bridge system and a method thereof comprising all the claims subject matter as discussed in the subparagraph 3 above, except for a voltage detector coupled to the first and second voltage buses.

Liu (Fig. 3) discloses a bus circuit in which a voltage detector (18) is connected to a voltage bus.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the voltage detector being connected to a voltage bus as shown in Liu into the bus bridge system of Khosrowpour and Nagakawa et al. for the purpose of determining the voltage on the voltage bus of the system.

6. Claims 14 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of prior art of record taken alone or in combination shows the bridge circuit including a NAND gate, first and second inverters and a transistor along with specific electronic connections as recited in the claims of 14 and 37.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chung (U.S. Pat. No. 6,617,879), Dathe et al. (U.S. pat. No. 6,798,188) and Chan et al. (U.S. Pat. No. 6,871,291) also disclose bus bridge systems each of which comprises substantially elements as recited in the claims of the instant application.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew V. Nguyen whose telephone number is (571) 272-2081.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2800.

MATTHEW V. NGUVEN PRIMARY EXAMINER

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